**Amendments to the Specification**

Please replace the paragraph beginning at page 8, line 6, with the following amended paragraph:

-- Figures 2A-2H depict stages in the fabrication of a trench structure in a semiconductor device using a "via first" dual damascene process. The process begins, as shown in Figure 2A, with the formation of a first barrier layer 202 containing silicon carbide and nitrogen over a first metal layer 204. The first barrier layer 202 may be formed by plasma enhanced chemical vapor deposition ("PECVD") methods with some flexibility provided in the selection of the chemical precursors. According to this technique, a variety of liquid or gas precursors that contain the methyl group may be used to form the silicon carbide barrier layer, as is well known in the art. For example, the silicon carbide layer may be formed by injecting an $SiH_x(CH_3)_y$ gas, where x is chosen in the range of ~~1 to 4, and~~ 0 to 3, and x+y = 4. Such methyl-containing precursors, known in the art as 3MS, 4MS, or 1MS,for example, provide satisfactory results. An inert gas such as Helium or Argon may be selected as the carrier gas. Nitrogen doping into the barrier layer results from providing a flow of an ambient gas, either ammonia ($NH_3$), nitrogen ($N_2$), or nitrogen oxide ($N_2O$). --

Please replace the paragraph beginning at page 8, line 6, with the following amended paragraph:

--The photoresist mask 216 is removed following formation of the via. A BARC layer (bottom anti reflective coating) (not shown) may then be deposited in the via to protect the bottom SiC barrier layer of the via from opening during trench etch (and having the underlying copper sputtered). [[***]]Then a second photoresist layer 220 is deposited to pattern and etch a trench. In this step as practiced in conventional processing without the nitrogen-free barrier, the photoresist in the via would be exposed to nitrogen present in the low-k dielectric layers 208 and 212 (from the nitrogen doped barrier layer). The anti-reflective layer (BARC - not shown) which, if present, is deposited immediately before the photoresist layer 220, and would not

prevent nitrogen present in the low-k dielectric layer from diffusing into and poisoning the photoresist 220 in conventional processing. Continuing with the process of the present invention, the second photoresist layer 220 is patterned and etched to form the trench 222 as shown in FIGs. 2I and 2J. Etching stops on the etch stop layer 210 to form the trench and via structure shown in FIG. 2J. In subsequent steps well known to those of ordinary skill in the art, the photoresist mask 220 is removed as well as the barrier layers (202, 206) adjacent to the metal layer 204. According to standard processing techniques, the via and trench will typically then be filled with copper by electrochemical deposition.--